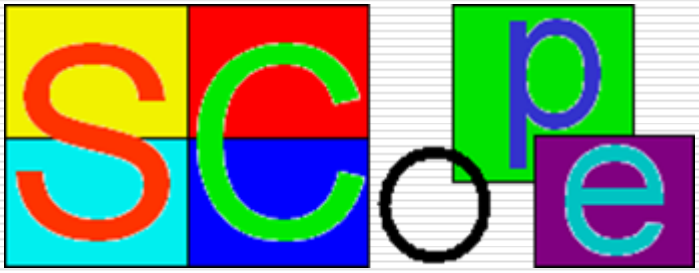

SCope: Efficient HdS simulation for MpSoC with NoC

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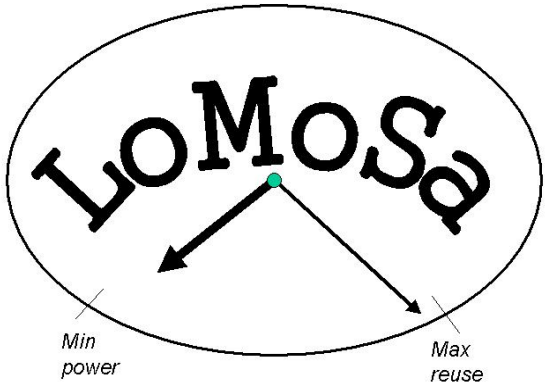
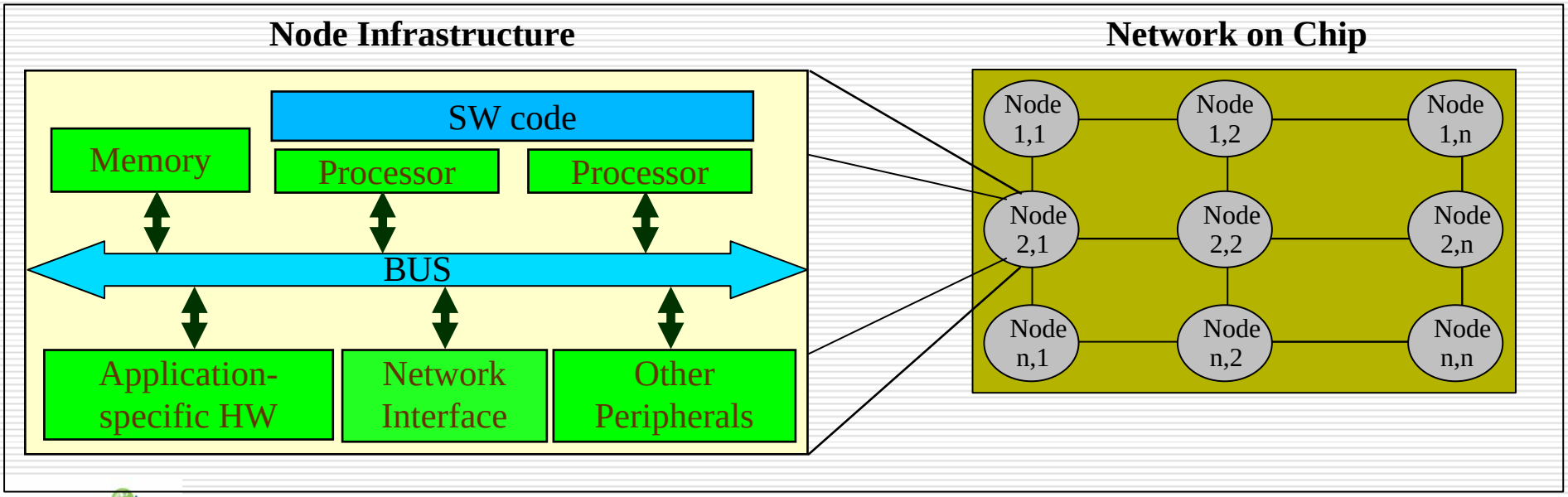
DS2



Motivation

- The microprocessor will be the NAND gate of the integrated systems in 2010
  - Alan Naumann, President and CEO, CoWare
  - DATE'07



Motivation

- Simulation will remain a fundamental design tool
  - Functional validation
  - Performance estimation
  - Design-space exploration
  - Design verification
  - ...

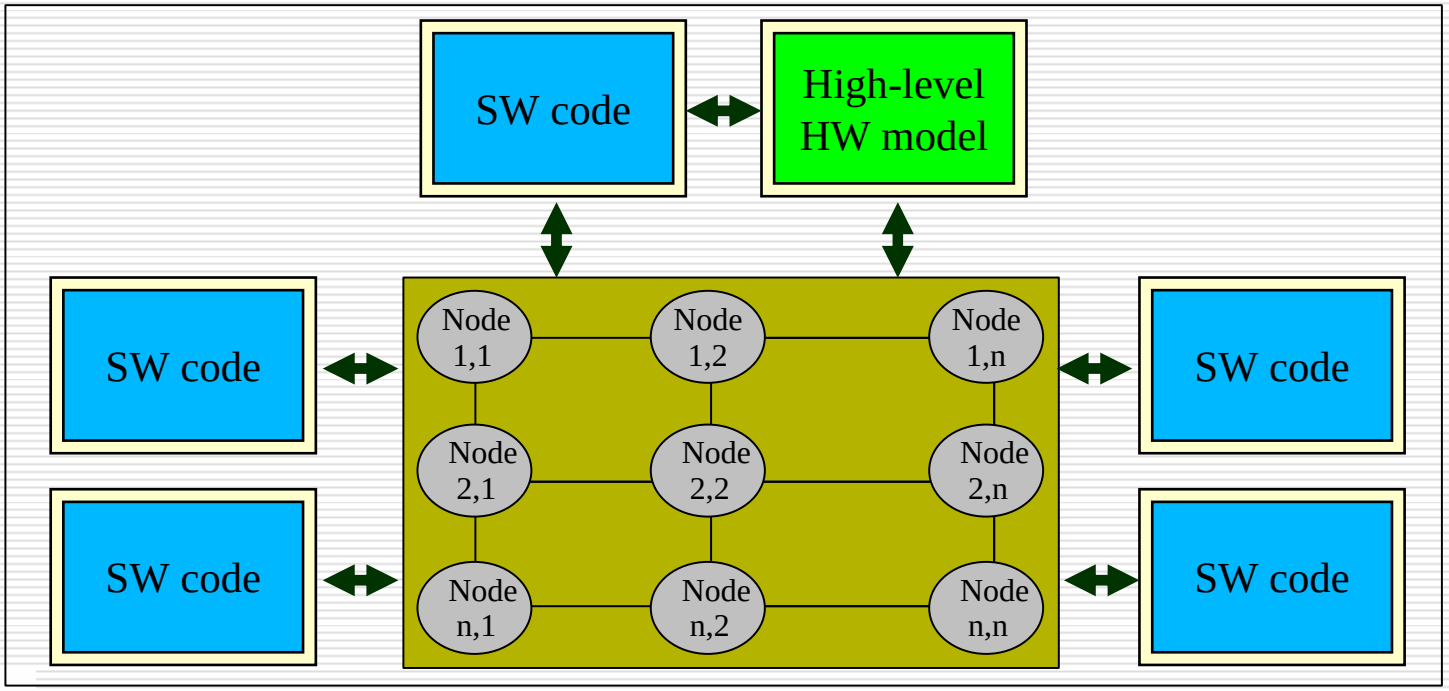
Motivation

- Current ISS(+TLM) is too slow for
  - Functional verification
  - Performance estimation
  - Design-space exploration

  - Only valid for final design verification
    - ISS+RTL(logic)

Motivation

- SW execution is only valid for
  - Initial functional validation
    - Temporal behavior missed



Contents

- SCope description
  - Goals
  - Features
  - Platform model
  - Power estimation
- Application example
- Conclusions

SCope: Goal

- HW/SW simulation platform for MpSoC with NoC
- Performance estimation
- Power estimation
- Fast
- As accurate as possible

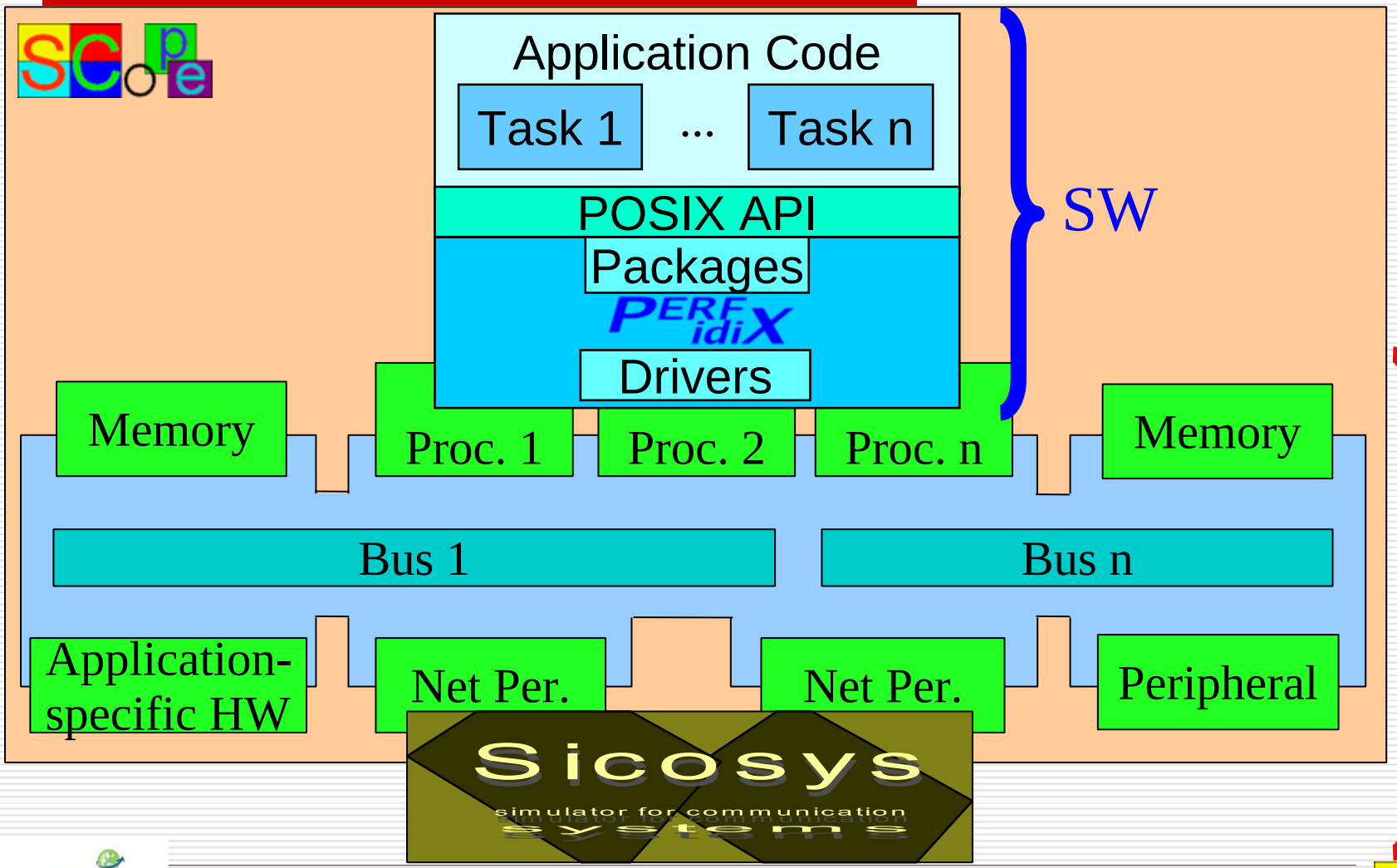
SCope: Features

- SW source-code simulation
  - Two orders of magnitude faster than ISS
- Abstract RTOS model
- Abstraction of the microprocessor
- Timed simulation
  - Performance estimation
- Power consumption estimation

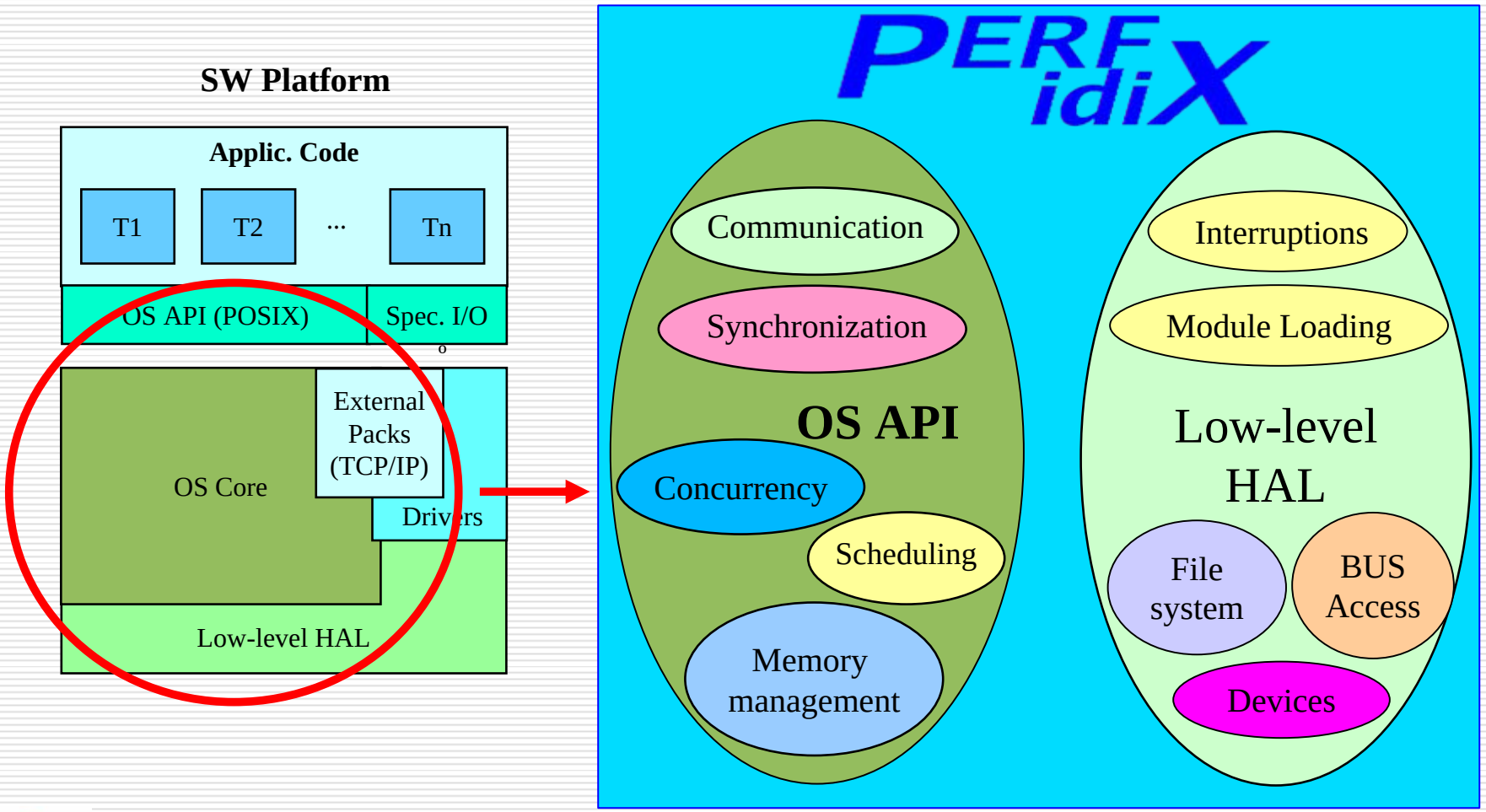
SCope: Features (cont.)

- HW TLM(RTL) models
- HW/SW communication
  - Interruptions
  - Drivers
- TLM2 Bus model
- DMA
- NoC Interface

SCope: Platform model



SCope: RTOS modeling



PERFidiX: HAL Modeling

- HW/SW communication
  - Drivers
    - Linux functions for drivers development
    - File system control and device management
  - Bus Access
    - Reading and writing
      - memory and peripherals
  - Interruptions
    - IRQ from HW platform
    - Interrupt managers and masks

PERFidiX: SW Packages

- POSIX-based RTOS allow inclusion of standard packages
  - Stack TCP/IP: lwIP
    - Reduced memory requirements
    - Several protocols implemented
      - IP, ICMP, UDP, TCP, DHCP, ARP, …
    - Uses a Ethernet driver model
      - Connected using the network simulator
    - Work in progress

PERFidiX: Execution time and Energy estimation

Dynamic Time & Power Estimation

Operation	Time	Total	Energy	Total
a = b + d ;	2+7 us	9 us	2+5 uJ	7 uJ
c = a*b ;	2+68 us	79 us	2+40 uJ	49 uJ
d = a;	2 us	81 us	2 uJ	51 uJ
if (c < 0)	20+18 us	119 us	20+10 uJ	81 uJ
a = c + 1 ;	2+7 us	128 us	2 + 5 uJ	88 uJ
Total seg.		128 us		687 mW

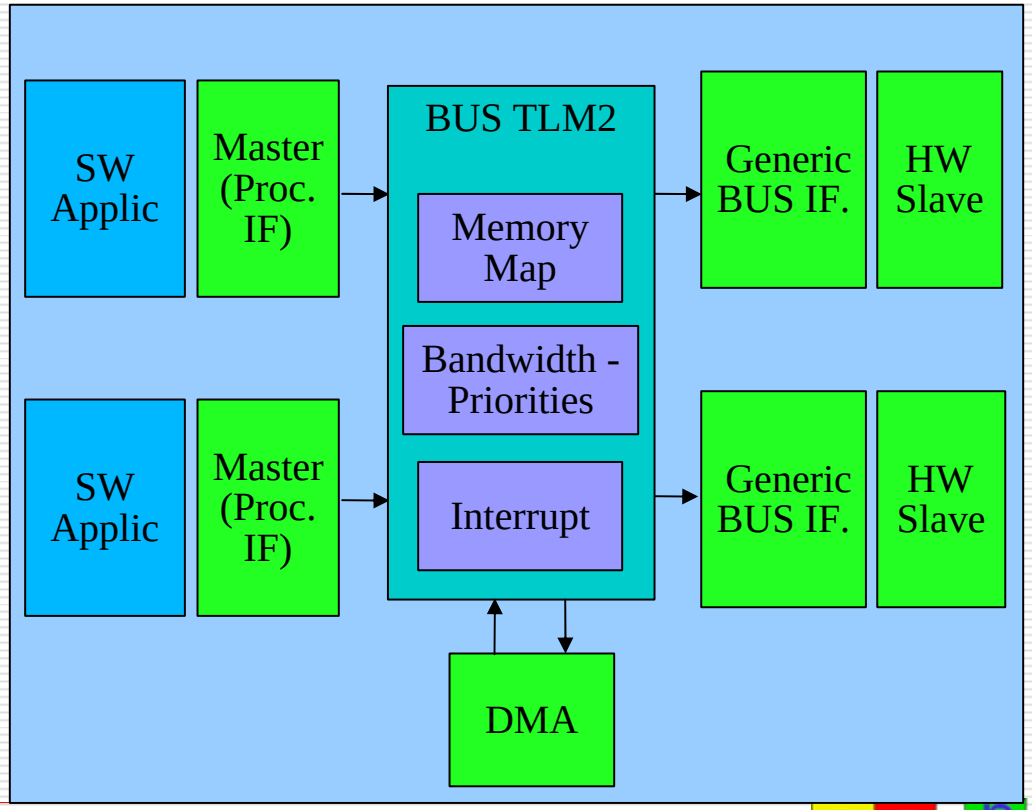
OPERATOR	Time	Energy
=	2 us	2 uJ
+	7 us	5 uJ
*	68 us	40 uJ
<	20 us	20 uJ
IF	18 us	10 uJ

PERFidiX: Power estimation

- Standard RISC processors exhibit stable power consumption per instruction
- Dynamic simulation allows estimating energy consumption
  - number of assembler instructions executed
  - energy cost per instruction
- Power estimation
  - energy/execution times
- Adaptive dynamic voltage-frequency scaling

SCope: BUS modeling

- Data Transfers
  - payload (faster than word by word)
- Interruptions
- TLM2
- Models
  - Several masters
  - Several slaves
  - Bus chaining
  - Stop / Abort



SCope: Generic peripheral interface

- Bus protocol management
  - Implements transport & send interrupt
  - Manages Stop and Abort operations
  - Waits corresponding time
    - bandwidth and delay
- Integrated using inheritance
  - Allows modifying protocol management in a specific peripheral
  - Protocol functionality integrated in the peripheral
  - Declare bus ports automatically (SC_EXPORT)

SCope: Specific Peripheral models

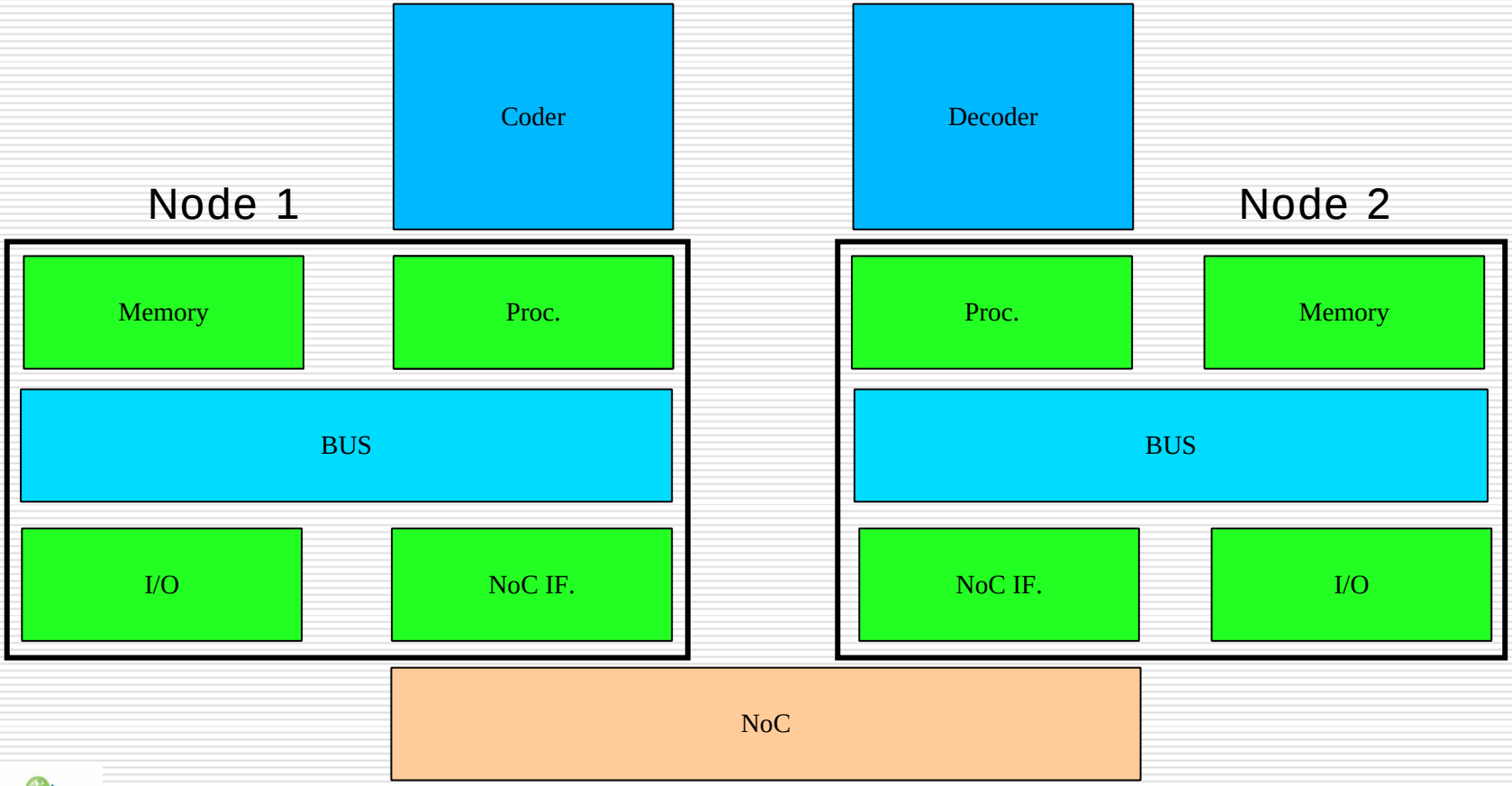
- Network Interface
  - Connects the bus and the NoC model
  - Acts as slave
  - Informs the processor through interrupts
- DMA
  - Master / Slave
  - Moves payloads between other peripherals
- Memory
  - Allows modeling bus loads of data transfers
    - processor-memory and DMA-memory

SCope: Network Modeling

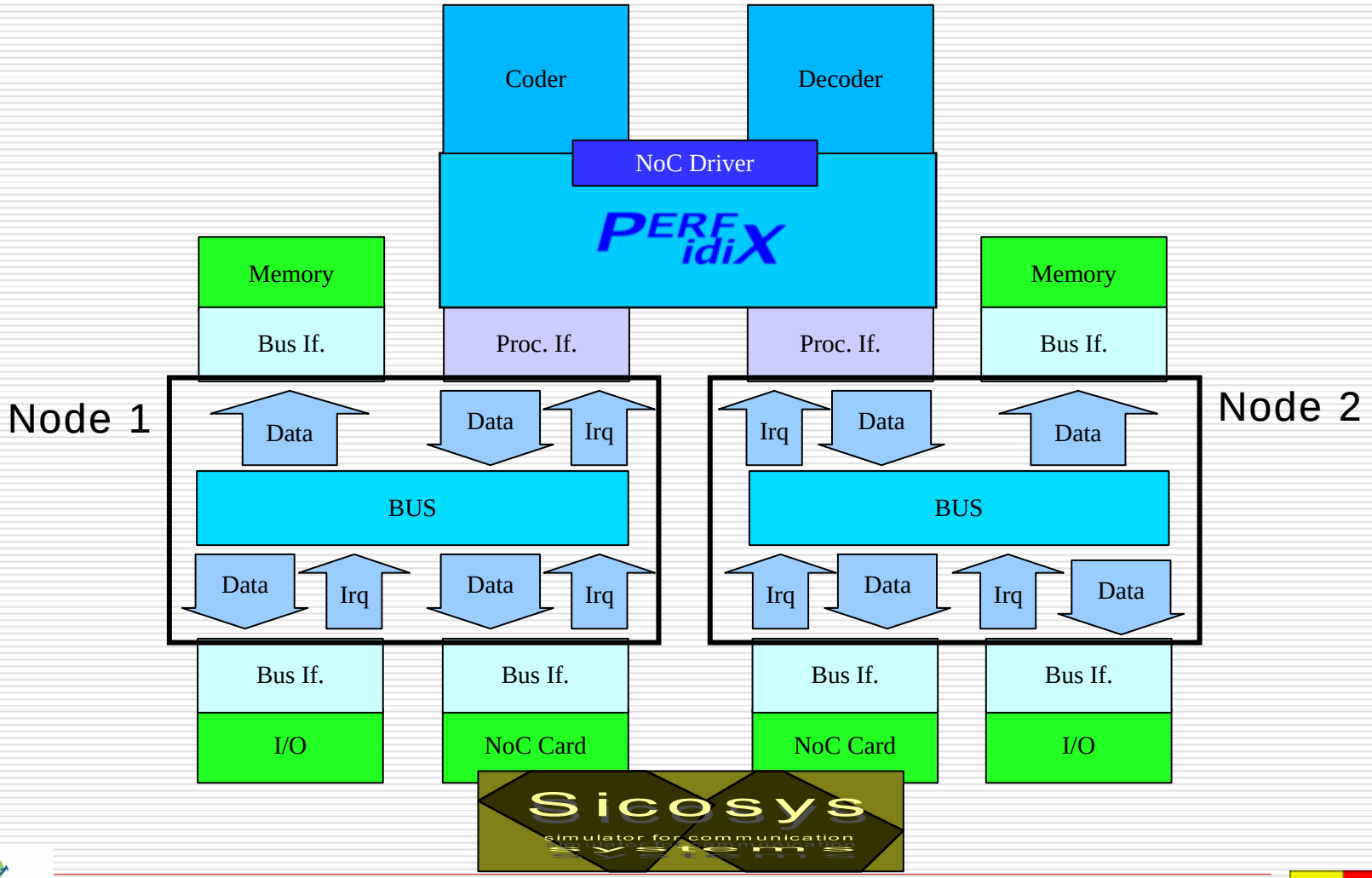
- Network on Chip simulator: Sicosys
  - University of Cantabria (UC-ATC)
  - Based on models of the NoC components
  - Several NoC configurations
- Integrated as a SystemC Thread
- Computes when packages are in the NoC
  - Otherwise Stopped

Example: Vocoder GSM

- Two nodes connected through a NoC



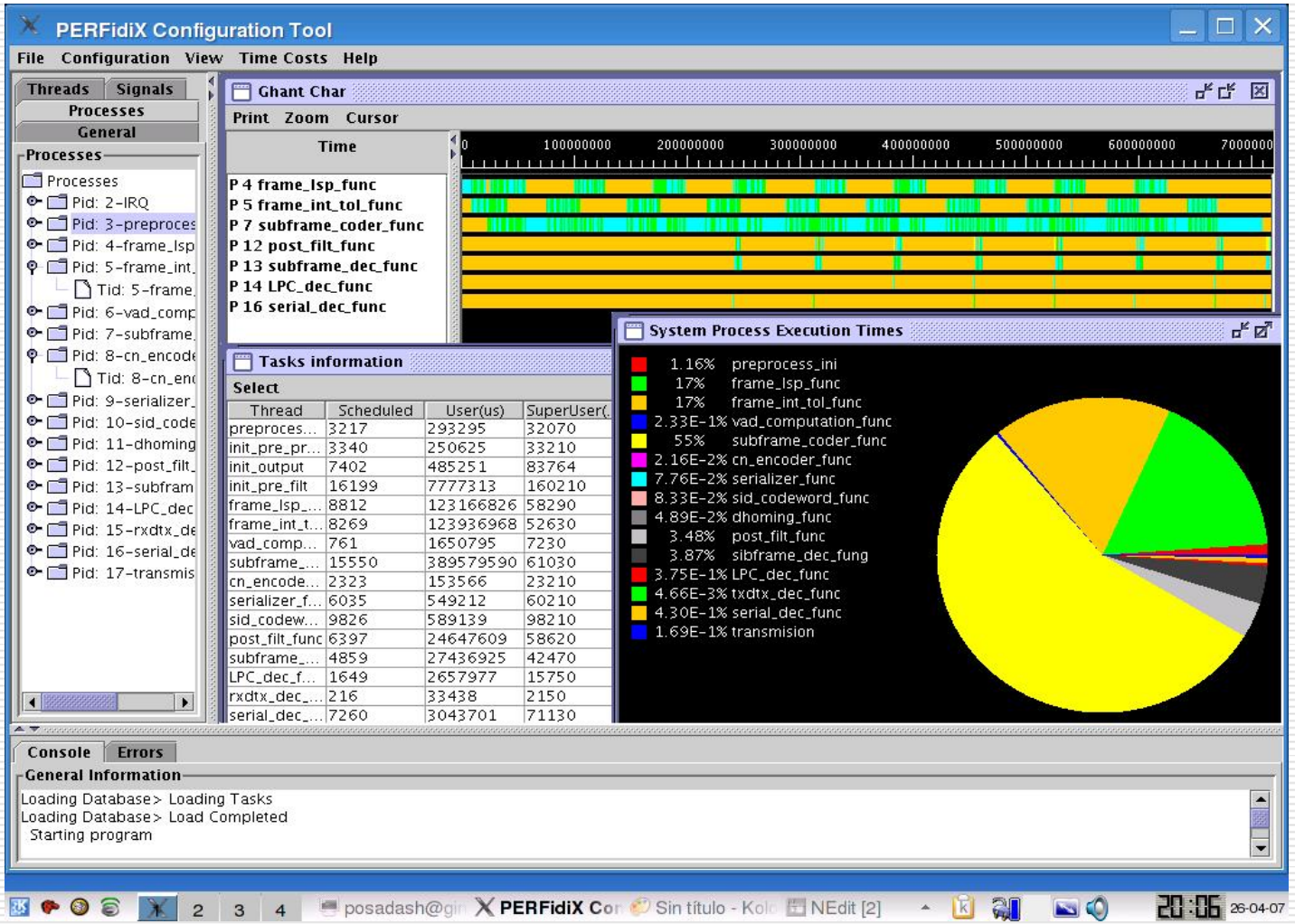
Example: Platform model



Example: Performance Analysis

- SW execution times
  - Thread statistics
  - Power consumption
- Bus statistics
  - Contentions
  - Conflicts
- Network
  - Delays
  - Latencies

Example: Performance Analysis



Conclusions

- SystemC
  - powerful framework for complex SoC with NoC modeling
- SCope
  - Multiprocessing SW simulation
  - SW power consumption
  - Platform modeling
    - Bus, DMA, AS-HW, Memory, NoC IF, ...
  - NoC simulation
    - Sicosis