SATURN Presentation

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Agenda

- Project Overview
  - Objectives
  - Consortium
- Saturn Design Flow
  - Code generation
  - Verification framework
- Demonstrators
- Conclusions

SATURN

- SysML bAsed modelling, architecTUre, exploRation, simulation and syNthesis **for complex embedded systems**
- SATURN's goal is to bridge the current gap between modelling and verification/synthesis in UML based designs of Embedded Systems that are equally composed of **HW and SW**
- In addition to this,
  - We are adding formal semantics of different Models of Computation for integrated modelling and verification environments
  - MARTE is being evaluated for its complementary application with SysML

Objectives

- To close the gap between **MDA-based modelling** and simulation by the integration of OMG **SysML** modelling tools with simulator-based run-time environments (RTEs)
- To bring SysML and MARTE into industrial application based on two real **industrial case studies** (Smart Cameras, broadband wireless telecom system) considering all facets of embedded systems design including system level design, RTOS, and hardware aspects
- To push European-based tool vendors and directly exploit project results into existing **commercial products**

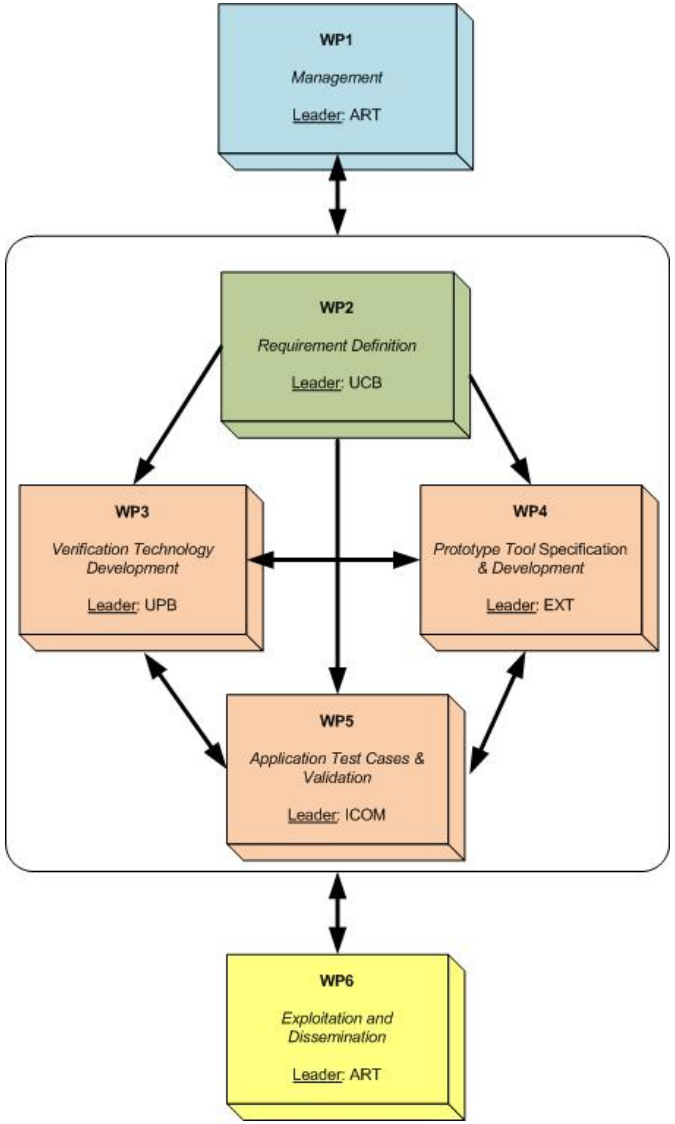
Consortium

- European-based tool vendors
  - Artisan
  - Extessy
- European system houses
  - Intracom Telecom
  - Thales Security Systems
- Research Centers
  - University of Paderborn
  - University of Cantabria

Project Implementation

- 3 technical WPs
  - WP3 Verification Technology Development
  - WP4 Prototype Tool Specification and Development
  - WP5 Application Test Cases and Validation
- WP1 Project Management
- WP2 Requirements Definition
- WP6 Exploitation and Dissemination

- Starting date: 1st January, 2008
- Finishing date: 31st December, 2010

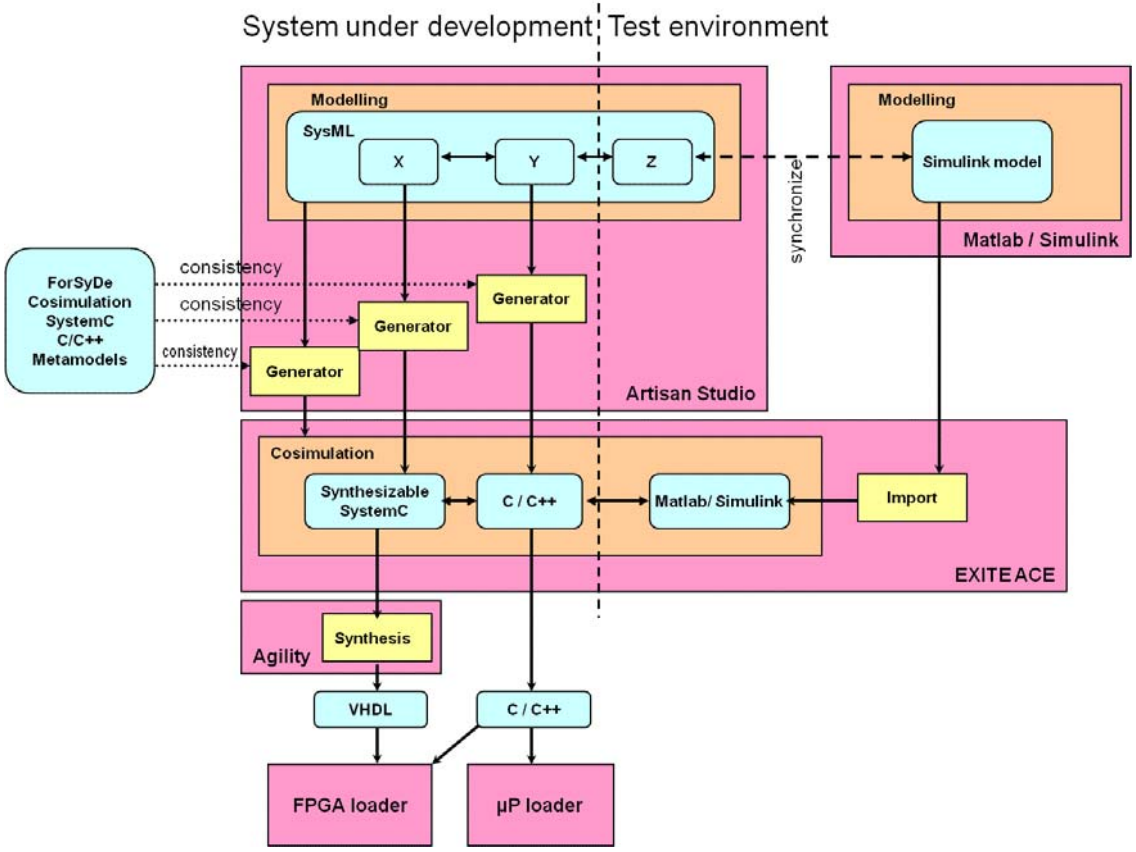


Saturn tools

- Plan is to allow users to input there design in to Studio in SysML
- Saturn profile for SystemC that enables SystemC specific constructs to be modelled.
- Code generation capability from Artisan Design Studio to Synthesisable SystemC along with standard Studio C/C++ capability
- Some modelling can be done in Simulink
- Extessy EXITE ACE tool enables co-simulation of the whole system
- The Synthesisable SystemC will be translated to VHDL for transfer to the FPGA
- Embedded SW in C/C++ will be compiled/loaded to the microprocessor element

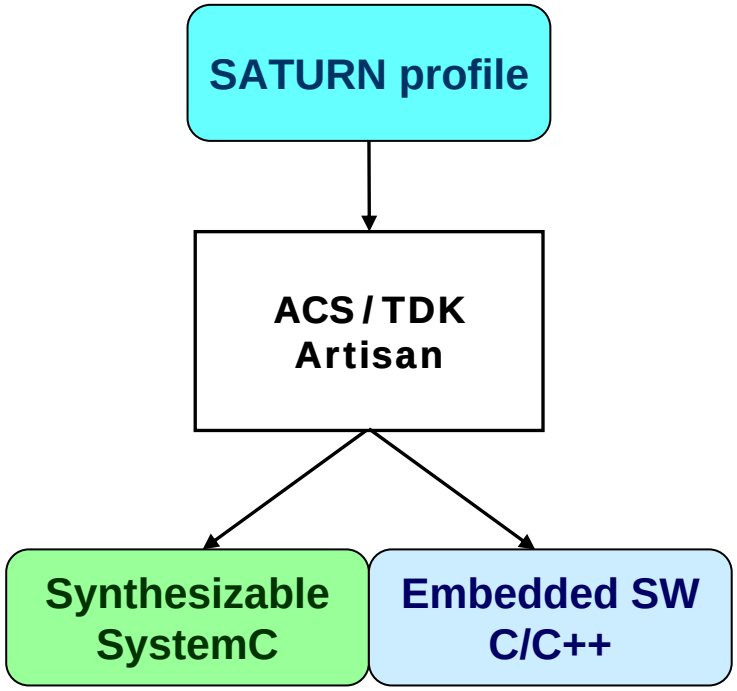
The SATURN Tool Chain

- Model generation, verification and implementation



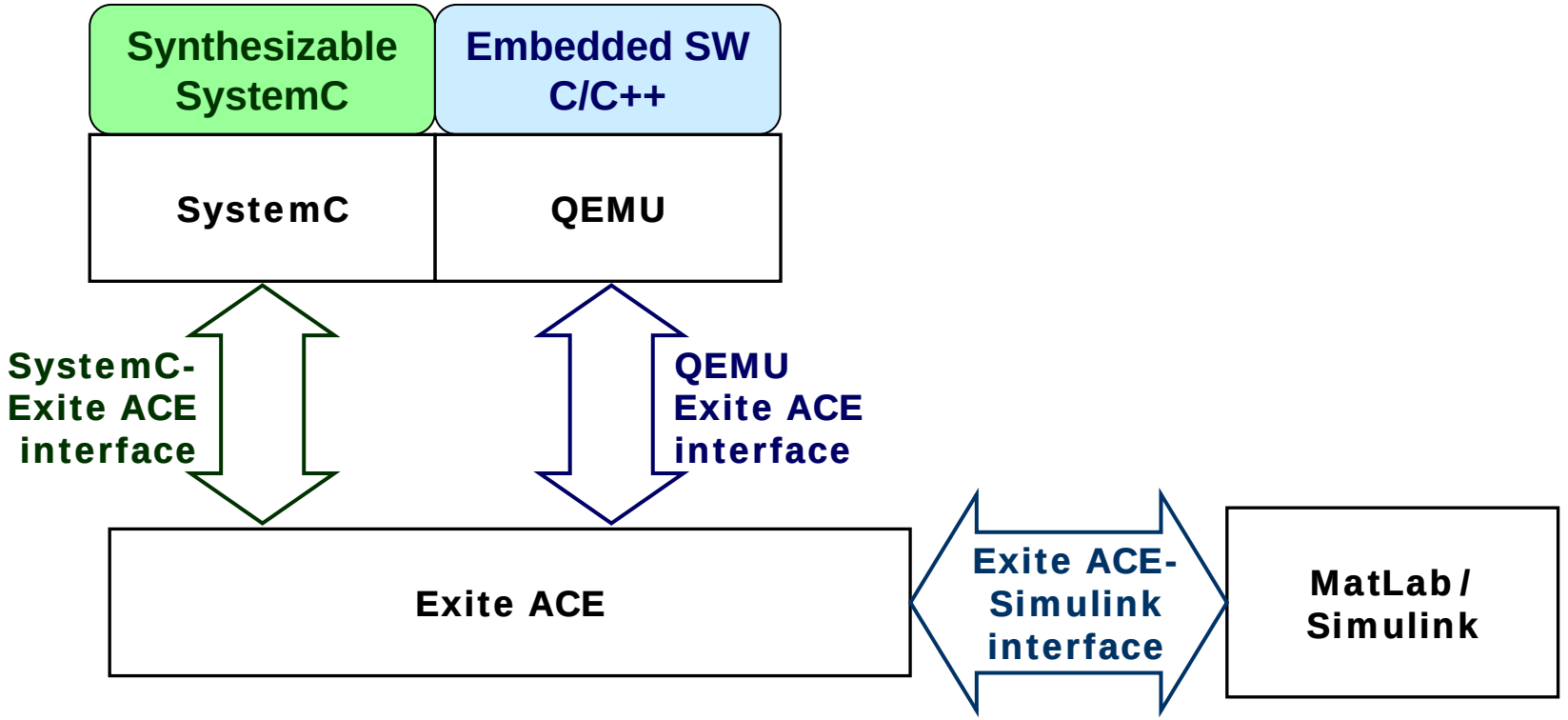
Model generation

- From SysML to HW & SW



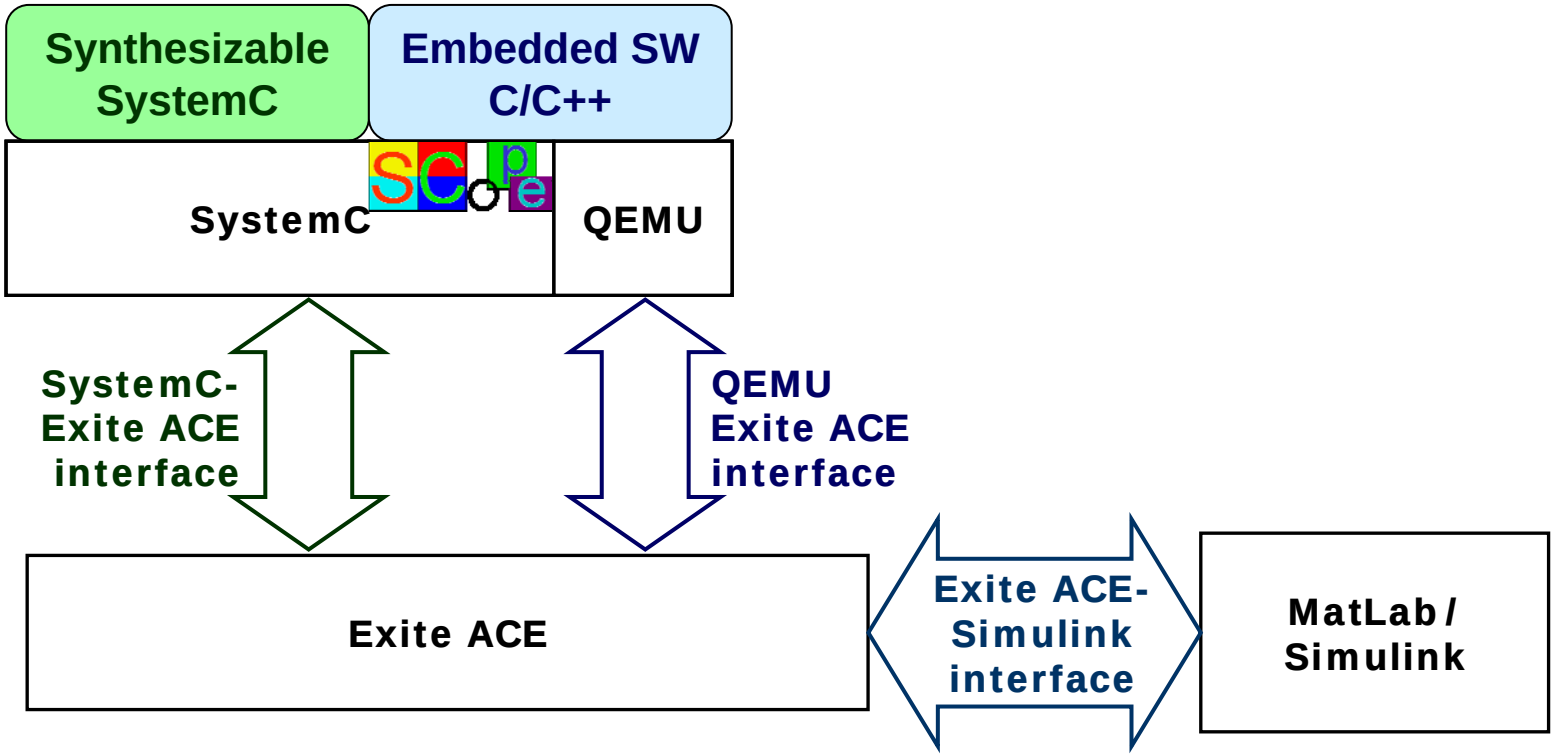
System verification framework

- Heterogeneous simulation framework



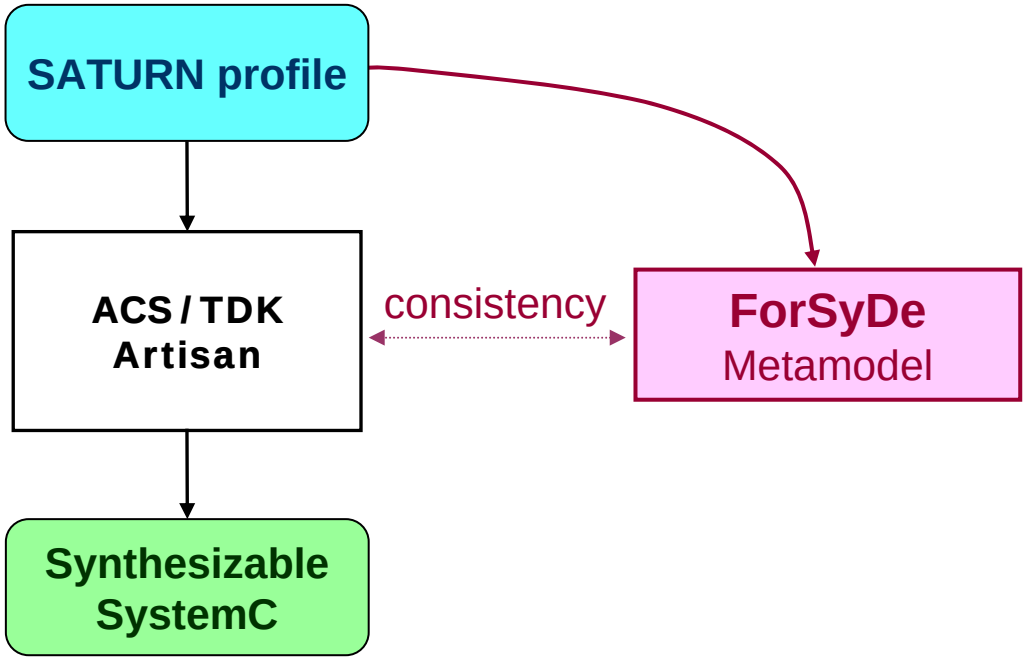
System verification framework

- Heterogeneous simulation framework



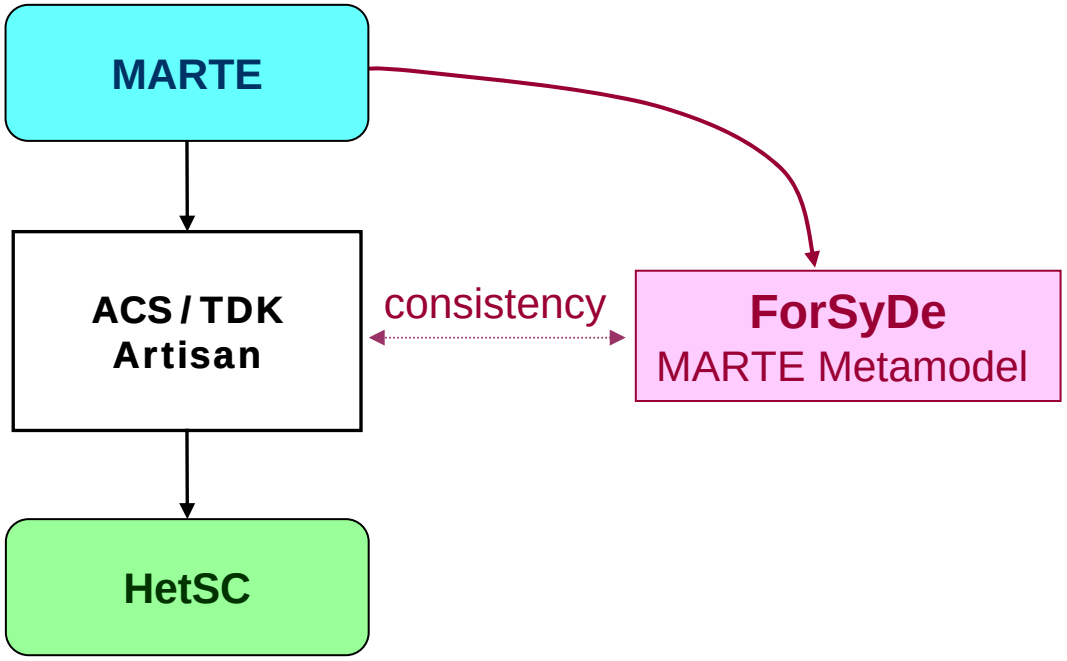
Formal support

- ForSyDe metamodel



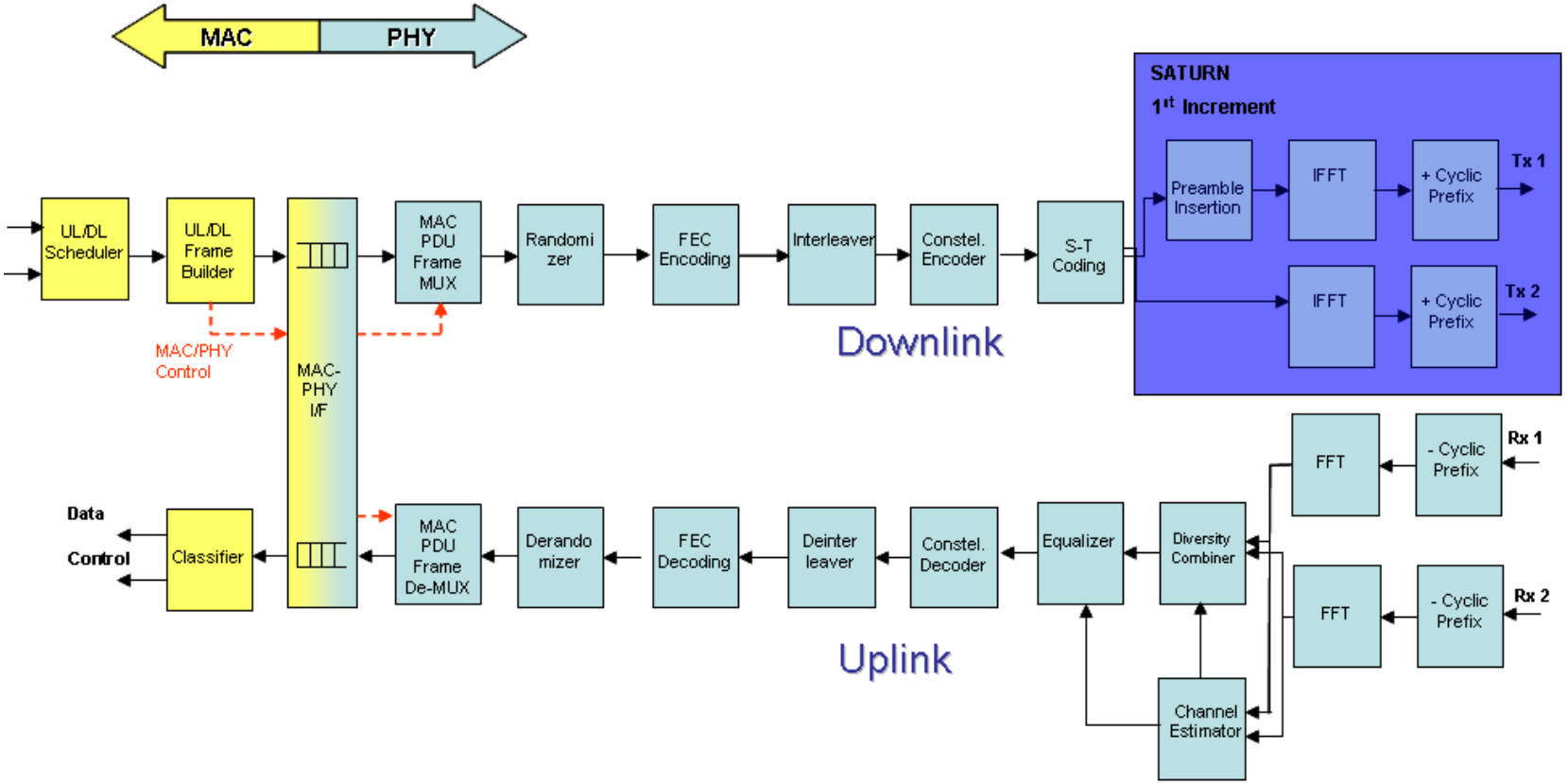
Additional research activity

- MARTE/SystemC interoperability



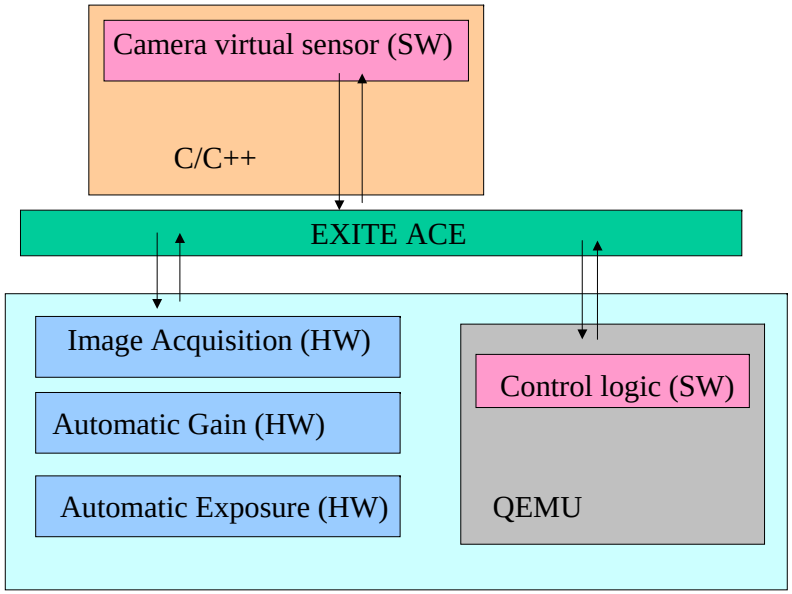
ICOM Demonstrator

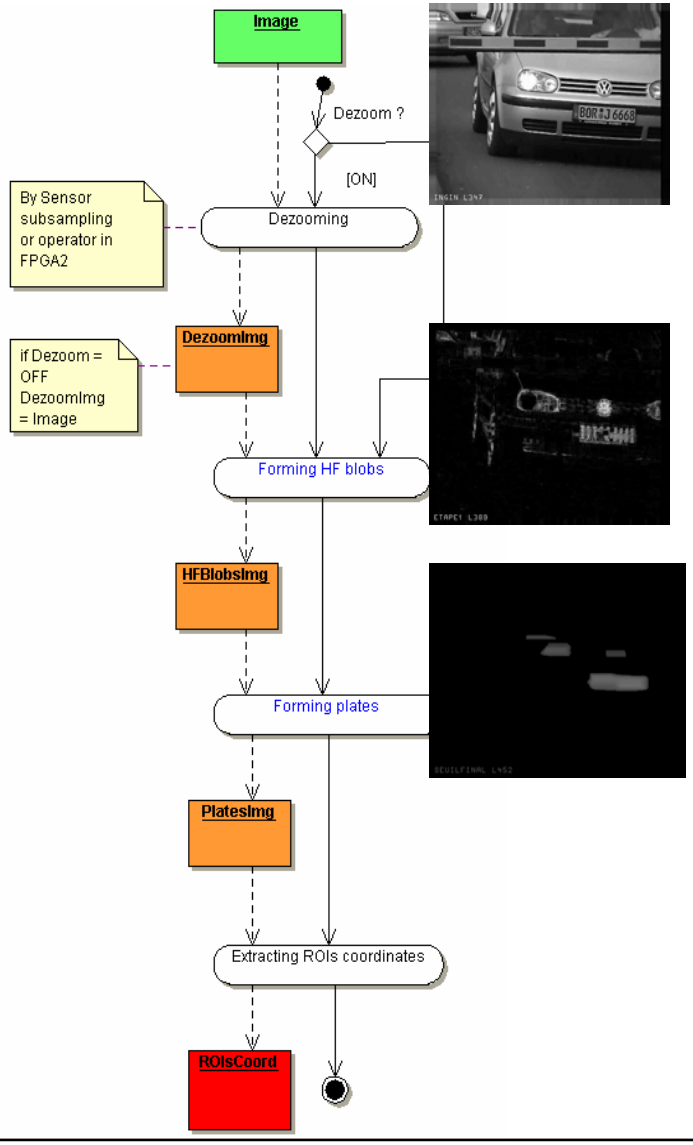
- IEEE 802.16e OFDMA Chain



Thales Demonstrator

- SmartCam
  - Licence plate recognition (pre-processing)





Conclusions

- Embedded Systems Design Flow
  - Using standard languages
    - UML/SysML/MARTE
    - SystemC
    - VHDL
    - MatLab/SimuLink

Conclusions

- Code Generation
  - UML/SysML/MARTE
  - SystemC
  - VHDL

Conclusions

- Embedded Systems Verification Framework
  - System specification
    - MatLab/SimuLink
    - SystemC/HetSC
  - SW
    - QEMU
    - SCoPE
  - HW
    - Synthesizable SystemC
    - VHDL

Conclusions

- Additional information
  - www.saturn-fp7.eu